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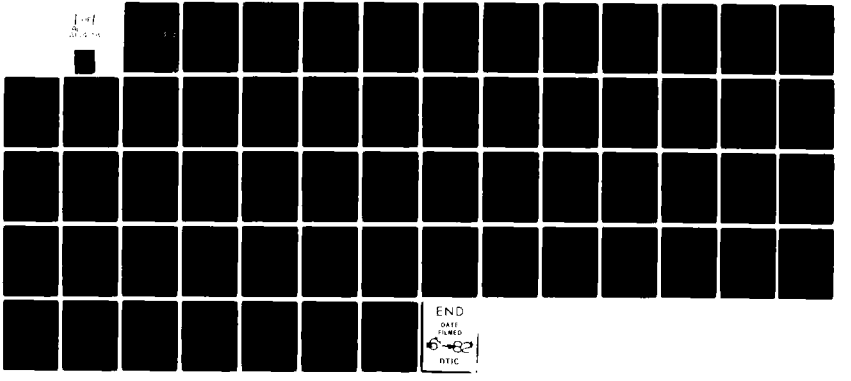

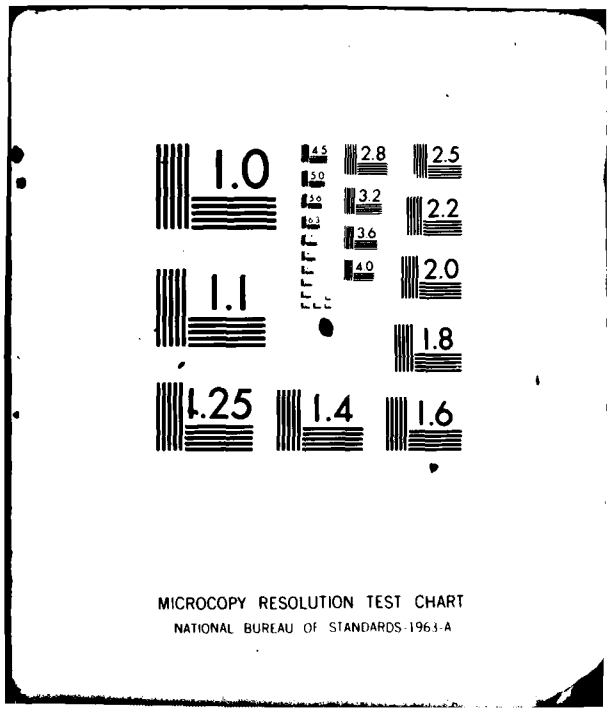
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DESIGN STUDY FOR A SEISMIC RESEARCH CENTER: HARDWARE CONFIGURATION

J. BERGER

TOPICAL REPORT

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20. ABSTRACT (Continue on reverse side if necessary and identify by block number)

The design of a seismic research center is considered. This system is to perform the tasks of the present SDAC and to meet the requirements of a seismic data center which can record and process the data from up to 50 NSS Mod II type seismic stations.

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ABSTRACT (Continued)

A design is developed consisting of four modules: a multi-microcomputer front end for communications and detection of seismic signals in the data stream; a recording mini-computer to archive the data and write the detection to disk; a network analysis computer to perform associations of events with detections; and a research computer to perform general scientific computing in a multi-user, multi-task environment. Specific hardware is recommended for each module and for a local network which will connect the machines to each other.

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I. INTRODUCTION

1.1 THE SEISMIC RESEARCH CENTER: GENERAL CONSIDERATIONS

This design study considers a program whereby the existing SDAC system can evolve into what will be called the Seismic Research Center (SRC). The design is primarily one for a research center as opposed to an operational data processing center which must routinely and reliably process real time seismic data with a set of fixed, well developed algorithms. The research nature of the new system will be stressed as it is clear that the manner in which many of the system functions of an operational Seismic Data Center (SDC) will be performed have not yet been worked out. The detection algorithms, the association processes, and the event location algorithms are but a few examples of areas in which much research is still needed. Thus, we see the SRC design as being strongly weighted towards a very flexible and powerful computational facility.

The system's flexibility is controlled both by the physical hardware configuration and by its programability. The physical configuration must be easy to change, e.g., by adding processors, peripherals, I/O channels, etc. These changes should be quickly and simply accomplished without major system interference, such as down time, reprogramming time, etc. In this respect, custom or rare equipment should be avoided as should obscure programming languages and operating systems.

The programability of the SRC depends upon the operating system (software) and upon the availability of an array of developmental aids such as editors, assemblers, compilers and, of course, higher-level languages.

Finally, the overall performance of the SRC system will depend upon its computational power. This includes the

processor speeds, the I/O bandwidths, the peripheral speeds and the interprocessor bus (or communications) speed. Clearly, the various CPUs and peripherals must be specified with a view towards their compatibility.

The specific tasks that the SRC must perform include:

1. To act as a research center for experimentation with selected seismic data sets.
2. To perform data services for external users - mostly writing special tapes of selected event waveforms.
3. To archive all incoming real-time data and some additional alphanumeric (A/N) data.
4. To perform research on automatic seismic event location (generating a bulletin) using real time data plus A/N data:
   A. To detect "signals" in the data stream and form the phase arrival file (PAF).
   B. To separate from the continuous data a signal waveform file (SWF) which contains all the "interesting" data to be kept on line for > one day.
   C. To associate "events" with arrivals and produce an automatic bulletin.

As stated earlier, we distinguish between an operational seismic data center which must receive and process routinely all incoming data and a seismic research center which can handle and process the real time data but is not so specifically designed. The differences in design mainly concern reliability and redundancy and the extent to which those characteristics dominate the design. There is nothing mutually incompatible between the designs of an SRC and SDC and indeed,

this design study will specifically address the requirements of an SDC but the emphasis will be upon a flexible research system. If so required, the SRC suggested in this study would be capable of performing all the tasks of an operational SDC.

1.2 SPECIFIC TASKS

The requirements of the SRC will include some time critical tasks. These principally are involved in handling the real time data. There are also numerous "off-line" or non-time critical tasks.

Time Critical Functions

- Communications Protocol
- Detection Processing
- Archival Storage
- Building PAF, SWF

Nearly Real Time Functions

- Secondary (Refined) Detection Processing
- Automatic Association
- Data Base Management

Off-Line Functions

- Visual Data Examination
- Data Services
- Discrimination Research
- Detection Research
- ?

The real time seismic data to be processed by the center controls the time critical parts of the system. For design purposes, we define a communications channel and a seismic channel as follows:

Communications Channel - A single modem connected to one station (or several) with a data rate of 4.8 kilobaud = 600 bytes per second (BPS).

Seismic Channel - A single bit stream from one component of ground motion. Typically there will be three seismic channels per station (see Table 1.1).

1.3 INPUT DATA RATES

The overall input data rates are, for design purposes, divided into two categories, the 1980 data rate and the "future" data rate. The former was specified by VSC personnel to be those stations and sample rates given in Table 1.2. The future data rate is simply that produced by 50 stations of the NSS Mod II type (Table 1.1) each operating over a 4.8 Kbaud communication channel. These overall data rates are outlined in Table 1.2.

1.4 HARDWARE CONFIGURATION

The overall block diagram of the complete SRC system is shown in Figure 1.1. The details of the system are discussed in later sections but the basic design as shown consists of the following four functional modules:

1. The Detection Microprocessor (DμP).
2. The Recording Processor (RP).
3. The Network Analysis System (NAS).
4. The Research System (RS).

The analogy between these modules and the parts of the existing SDAC is close and intentional so that an evolutionary, step-by-step implementation of this design can be accomplished.

TABLE 1.1

SEISMIC DATA RATE (NSS MOD II)

	Period Band	Sample Rate	BPS
Each component of motion is divided into three signals of differing frequency response	SP	40	80
	MP	4	8
	LP	1	2
			90
			x 3 components
= 270 BPS per station			

TABLE 1.2

SEISMIC DATA FLOW AT THE SRC

1980		Future	
1 HF @ 120 BPS =	120 BPS	50 Stations 3SP @ 80 BPS	240 BPS
30 SP @ 80 BPS =	2,400 BPS	3 MP @ 8 BPS	24 BPS
33 SP @ 40 BPS =	1,320 BPS	3 LPC @ 2 BPS =	6 BPS
3 SP @ 20 BPS =	60 BPS		270 BPS
33 MP @ 8 BPS =	264 BPS		x 50
73 LP @ 2 BPS =	46 BPS		13,500 BPS
	4,310 BPS	(HSS RATE =	13,000 BPS)

COMMUNICATIONS

1980		Future
11 4.8 Kbaud modems for NSS stations	52.9 Kbaud	50 x 4.8 Kbaud
1 4.8 Kbaud for ALK	4.8 Kbaud	
1 4.8 Kbaud for PWY	4.8 Kbaud	
1 9.6 Kbaud for NORSAR	9.6 Kbaud	
	72.0 Kbaud	240 Kbaud
	= 9 Kbytes/Sec	= 30 Kbytes/Sec

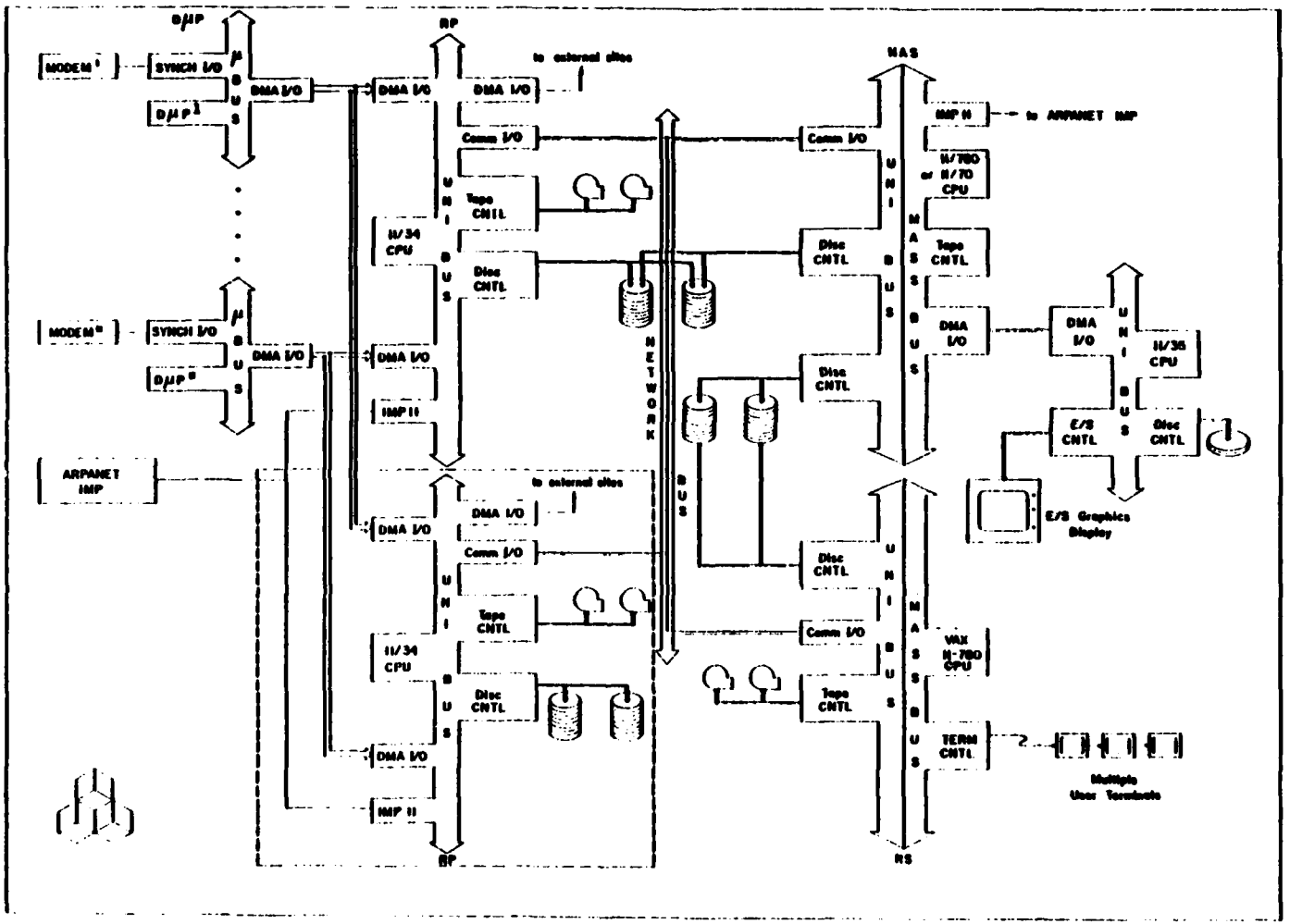


Figure 1.1. Proposed seismic research center.

Each of these modules will be discussed in detail in later sections, but we summarize those hardware changes in the present SDAC system which are recommended:

1. Elimination of the CCP.
2. Replacement of both IBM 360/40s.

There are several factors which ab initio point us toward Digital Equipment Corporation (DEC) hardware as vendor for the replacement hardware. Principally, these are:

1. The existence in SDAC of one DEC PDP 11/70.
2. The existence in SDAC of the Evans and Sutherland graphics system which utilizes a DEC PDP 11/35.
3. The LL-ASG design for the SDC which is built around DEC 11 series equipment.

It should be clearly stated that in our view, this type of equipment is highly suited for these purposes and would likely be chosen even if these factors were not taken into consideration. The 11 series of DEC computers offers an extremely broad range of compatible midi, mini and micro computers. The company is well-developed, the product line stable, popular and competitive.

With these comments in mind, we will not consider, in this report, products outside this line, with the exception of the microprocessor front end. Even here its compatibility with the DEC 11 series will be an important factor.

II. DETECTION MICROPROCESSOR

2.1 DESIGN PHILOSOPHY

It is clear that at a minimum, each communication channel (modem) will need a separate interface to the RP. A possible configuration of the RP and DP might be simply a CPU with many synchronous I/O ports doing all the protocol handling and detection processing sequentially.

The problem is one of processor loading. If we estimate the time that the bus is occupied by simply writing the CW data to tape and some subset of this data to disk files, we find this will likely take up 30 percent of the available time for the "future" data rate. Add to this the interrupt handling of, say, 50 synchronous I/O ports and it is easy to see that even if the CPU is very fast, the machine will be unacceptably loaded merely performing these simple tasks without any detection processing.

The best way, in our opinion, to alleviate these problems is to impart as much intelligence as possible to the I/O interfaces. Obviously, they can handle the communication protocol, buffer the data, and transfer it into memory via DMA. But why not also do some reformatting and even detection processing in this "interface"?

The design we suggest in fact takes all of these tasks away from the RP and places them in the N front end detection microprocessors (DμP). These DμPs will each have several tasks to perform:

1. Handle communications protocol (possibly full duplex).
2. Process the data stream for "arrival" detections.
3. Form a signal arrival file.
4. Convert input data into a common format.

5. Possibly communicate with remote stations via full duplex for control functions.

6. Upon command transfer data blocks via DMA into RP memory.

2.2 MARKET SURVEY

We have conducted a market survey of microprogrammable microprocessors and microcomputers. Our findings are summarized in Appendices A and B. We have examined the available device specifications for the purposes of a DμP with particular emphasis on:

1. Speed
2. Programability
3. Availability
4. Cost (including development).

We seriously considered only "off the shelf" microcomputers as we believe that the cost of developing a microcomputer from microprocessor and other chips to be not worth the cost. It may be that when the specific functions of this DμP are completely determined, and the algorithms it must perform are decided, a more specialized machine would be justified, but at the outset flexibility in this part of the system should be stressed. Thus, we put great emphasis on speed and ease of programming. These considerations directed our choice to two candidate microcomputers, the Plessey Miproc-16 and the just announced DEC LSI11-23. Their salient features are outlined in Table 2.1.

2.3 MICROPROCESSOR LOADING

In order to estimate the expected microcomputer processing load that will be applied by the specified data rates,

TABLE 2.1

DμP

	Plessey Miproc-16	DEC LSI 11-23
Technology	Shottky, bipolar	NMOS
Data word, bits	16	16
Instruction, bits	16	16, 32, 48
Clock	4 MHz	
Add time, register to register	0.250 μs	1.8 (est.)
Number of instructions	180	80
Number of registers	4	8
Hardware F.P.	(In development)	Yes
RAM		
Capacity	64K	256 KB
Cycle time	100 ns	500 ns
PROM		
Capacity	64K	64K
Cycle time	70 ns	400 ns
I/O		
Word size	16	16
Number of channels	256	Bus
Maximum I/O rate	3.0 MBPS	1.67 MBPS
SOFTWARE		
Resident assembler	No	Yes
Cross assembler	PDP11	
Monitor or executive	Yes	RT11, RSX11M
Higher level language	PL-Miproc	FORTRAN, BASIC
Price:	$2K, 1976	- , 1979
Comments	Fastest	Easiest to program.

we have constructed a hypothetical processor sequence for timing purposes. It consists of three distinct parts:

1. Communications handling (interrupt driven).
2. Detection processing and reformatting.
3. DMA transfers to the RP (interrupt driven).

We use an average instruction time (average of add and hardware multiplying time) of 0.85 μsec for the Miproc-16 and 3.9 μsec for the LSI11-23. Our estimate of the time required to execute this sequence of operations on each processor is given in Table 2.2.

If the estimates in Table 2.2 are realistic, we see that either microcomputer could handle the job easily, perhaps even handle more than one communication channel. Alternately, considerably more computing could be performed in this module. In particular, more sophisticated detection algorithms may be desired or more than one running simultaneously may be advantageous. Further, data compression schemes, if they can be devised, would be performed in these "front-end" processors. In general, the more computational power that can be packaged in the front end, the more flexible the overall system will be.

The fundamental trade-off between these two machines is speed versus ease of programming. The Miproc-16 is without doubt one of the fastest microcomputers available on the market today. (It is available in a "Mil-Spec" version.) However, its programming language is unique, which is a drawback, even if it is a relatively powerful language. The development system used with this machine could easily be any DEC 11 series machine since Plessey supplies a cross-assembler that allows programs to be written and somewhat debugged on the DEC machine and then the Miproc-16 instructions are formed with the cross-assembler and down-loaded into the Miproc-16. Thus, the system is fairly compatible with the rest of the SRC system.

TABLE 2.2

ESTIMATES OF PROCESSING LOAD ON EACH CANDIDATE DμP
(UNLESS NOTED, ALL TIMES ARE IN MICROSECONDS)

	Task	Miproc-16	LSI11-23
1.	Interrupt	0.55	6.5
	Register Save	1.375	
	40 Instruction Interrupt Service Routine	34.0	160.0
		36.0	166.5
	x 300 Interrupts/Sec	10.8 ms	50.0 ms
	Load	1.0%	5.0%
2.	500 Instructions per each SP Input Word		
	500 x 3 x 4 = 60K Instructions/sec	51.0 ms	234.0 ms
	Load	5.1%	23.4%
3.	Interrupt	0.55	6.45
	Register Save	1.375	
	40 Instruction Routine	34.0	160.0
	DMA Transfer @ 600 KB/Sec	1000.0	1000.0
	Load	0.1%	0.12%
	TOTAL LOAD	6.2%	28.5%

The LSI11-23, on the other hand, is a genuine member of the DEC 11 series product line sharing common instruction sets, operating systems and higher level utilities. Thus, this type of DμP would be the easiest to integrate into the system.

2.4 THE CCP

The current hardware configuration at SDAC routes all data through the CCP before transmission to the IBM 360/40A DP. This has several drawbacks:

1. The CCP is a custom-designed machine. Hardware and software developments are very difficult and time consuming.
2. There is no "development" system. All software must be written and debugged on the operational machine.
3. Programs developed for the CCP are non-transportable.

Basically, there is no reason to include the CCP in the design we envisage. All the functions it is presently performing can be handled efficiently by either the DμPs or the Recording Processor.

III. THE RECORDING PROCESSOR

3.1 RP TASKS

The basic function of the RP (or both RPs, if redundancy is desired) is to archive the data being processed through the detection microprocessors. A requirement to archive all the incoming data is coupled with the requirement to store some subset of this data so that it may be accessable by other modules of the system in near real time. Thus, we will speak of off-line archival and on-line formation of what is termed the Phase Arrival File (PAF), the list of all detections discovered by the DμPs and their relevant parameters plus a signal waveform file containing a subset of the waveform stored in the archives. The specific tasks to be performed by the RP are:

1. To poll the DμPs periodically and transfer data blocks to memory.
2. To format and record all data and detections.
3. To format and write the PAQ and the SWF.
4. To communicate with the ARPANET.
5. Possibly to communicate with other locations to send subsets of the real time data elsewhere.

3.2 DATA ARCHIVING

We consider magnetic tape as the only practical media on which to archive all the data, at least at present. Currently there are "off-the-shelf" magnetic tape systems for the DEC 11 series machines available utilizing 1600 BPI, 75 IPS and 125 IPS mag tape drives. (6250 BPI drives will probably also be available within a year.)

For the on-line data files, disk storage modules are the only practical systems available now. These units are

readily available from many sources and provide the rapid random access entry needed for this application.

The load on the RP imposed by Tasks 2 and 3 will be caused primarily by the bus use of the recording peripherals, the mag tape and disk drive. Assuming 5 Kbyte data blocks (one second of network data at the 1980 data rate), this load is estimated as follows:

Task 2:	Tape 1600 BPI, 75 IPS	
	Start up	5 ms
	5 Kbyte data block	42 ms
	0.6 inch IRG	8 ms
	Stop	5 ms
		60 ms
Task 3:	Disk	
	Average positional seek	28 ms
	Average rotational latency	8.3 ms
	5 Kbyte data block	6.2 ms
		42.5 ms

Thus, to archive on tape and write to disk all data will take 102 ms/second representing a 10 percent processor load for the 1980 data rate. For the future data rate this will increase by approximately three to produce a 30 percent processor load.

The capacity of magnetic tape, formatted in a variety of ways, is given in Table 3.1. It is clear from the tape consumption figures that with the 1980 data rate 6,250 BPI drives are highly desirable and by the time of the future data rate, they are almost a necessity.

TABLE 3.1

ARCHIVE TAPE CAPACITY
2,400 FOOT REELS

Block Size	1,600 BPI (0.6" IRG)	6,250 BPI (0.3" IRG)
500 B	15.75 MB	37.98 MB
2 KB	31.15 MB	92.88 MB
4 KB	37.14 MB	122.58 MB

TAPE CONSUMPTION
4 KB/BLOCK

	1980	Future
1,600 BPI	2.06 Hours	40 Minutes
6,250 BPI	6.81 Hours	2.2 Hours

Assume 15 percent overhead for headers, etc.

3.3 ON-LINE DATA BASE

The requirement for an on-line data base is more problematical. At the 1980 data rate, data accumulates at the rate of 432 MB each day. At the future data rate, the daily accumulation becomes nearly 1,300 MB! Just what should be written to disk files needs careful consideration. The possibilities are:

1. All data.
2. Only a subset of detected waveforms.
3. All data, but in a "compressed" form.

The simplest and most straightforward approach is the first. Table 3.2 compares the capacities of a bank of eight 300 MB storage modules when all the data and 25 percent of the data is saved. The principal object in keeping several days (or more) of data on-line is to await the arrival at the center of arrival picks and event locations (alphanumeric) data) from other centers. This may take a week or more. We note, in passing, that in the final analysis the only signal waveform data of interest is the signal waveforms from the seismic events. Thus, the "ideal" SWF would contain for each station:

High frequency phases; 3 SP channels 10 sec of 80 BPS	= 2.4 KB
All phases; 3 MP channels 100 sec of 4 BPS	= 12.0 KB
Long period; 3 LP channels 1,800 sec of 1 BPS	= 5.4 KB
For each event at each station	19.8 KB
Times	50.0 stations
So a network event file	= 1 MByte

TABLE 3.2

RP

SWF AND PAF DISK FILES

EPOCH	1980		Future	
Accumulation	25%	100%	25%	100%
Input Rate	1.25 KBPS	5 KBPS	3.75 KBPS	15 KBPS
Daily Rate	108 MB	432 MB	324 MB	1296 MB
Capacity of a bank of 8, 300 m byte disk drives (88 percent formatted capacity)	19.5 Days	4.9 Days	6.2 Days	1.6 Days

The estimates of Chinnery and North (1975) suggest that there are about 24 earthquakes with $M_s \geq 4.0$ each day. Hence, this "ideal" SWF would accumulate at the rate of 24 MB/day versus 1,300 MB/day of all the data. This comparison simply emphasizes the potential gains to be achieved with better detection algorithms and network processing.

The third method of on-line data storage, utilizing data compression, is an area where little is known but where research could potentially be quite rewarding. The idea of data compression is based on the following observations:

1. Data is sampled in the field and transmitted at the highest rate ever needed. Most of the time the data is over sampled.

2. Data is sampled with a 16 bit data word. Most of the time many bits are redundant -- they do not change from sample to sample.

It seems as if one could make use of these facts in a processing scheme to greatly reduce the number of bits needed to represent the data stream and hence greatly reduce the data storage problems.

3.4 RP HARDWARE

The specific hardware we suggest for this application is a PDP11/34 acting as the RP CPU with 1,600 BPI 75 IPS tape drives or 6,250 BPI drives as soon as they become available, a bank of eight 300 Mbyte disk storage modules, and DMA I/O ports for communication with the DμPs. Since only one DμP is communicating with the RP at one time, this link could be multiplexed through a single DMA channel into the RP. The trade-off is basically between the costs (and practical limitations on number of units) of DMA ports versus the cost of development of a multiplexed bus. For upwards of ten channels,

the DMA port per channel is probably the most cost effective. For more channels, a multiplexed scheme is probably desirable.

Shown in the design of Figure 1.1 is an IMP11 UNIBUS interface to the ARPANET IMP. This peripheral will allow the RP to communicate with the ARPANET, receiving or transmitting data over this channel. If there is a need to communicate over regular telephone lines, say to send some of the data elsewhere, additional DMA, synchronous I/O ports can be easily added. Considering that the archival and disk file writing tasks will represent only a 10 percent CPU load for the 1980 data rate, considerable bus and CPU processing time is still available for other tasks.

The communication I/O port to the local processor network will be discussed in detail in Section VI. Suffice it to say, there will be such a network in this design so that all modules in the SRC can communicate easily and at a high speed with one another.

Finally, the matter of reliability and redundancy is not addressed in great detail in this design study. Again, the research nature of the system is stressed and not its operational characteristics. However, if it is a requirement to achieve extremely high reliability, two identical RPs can be configured so each has access to the data stream from the DμPs. Either both systems could operate all the time, or more practically, a second RP system could perform other tasks such as data services in the background of a foreground/background type of operating system (such as DEC's RT-11 operating system). When a system fault occurs on the primary system, a device such as a "watchdog" timer could interrupt the secondary system, switching it immediately into the foreground process which could be the RP task. It would only be necessary to keep a mag tape loaded and on-line and a disk drive in reserve for this task.

IV. NETWORK ANALYSIS SYSTEM

4.1 NAS TASKS

The functions of the NAS are basically the same as those of the Network Event Processor (NEP) in the present SDAC. The data sent to the system are the detections of the DμP's stored by the RP in the Phase Arrival File (PAF) and the Signal Waveform File (SWF). The output from the NAS consists of the daily event bulletins and the Event Waveform Files (EWF).

In the performance of these functions, the NAS will access the disk files created by the RP and will act as a host to the analyst's graphic stations. In the present SDAC configuration, the NEP does not keep up with the data flow for a variety of reasons. Perhaps the chief reason for this is the poor global seismic coverage of the current real time data stream. This means that before the association process can make much headway, arrival times and event locations from other sources (i.e., NEIS, UK and Canadian arrays) must be obtained and it may be in excess of a week before this occurs. Thus, the NEP must work from the archived tapes rather than from a disk file and the tape to disk transfer is slow. A further cause of delay in the processing is the necessity of intervention by the analyst via the E&S graphics station but, here again, it is our opinion that more complete seismic coverage would speed up this process.

It is clearly desirable to make the on-line data span as much time as possible so that picks from external arrays and networks can be added to the PAF without the necessity of mounting the archive tapes as happens in the present SDAC operation. The total amount of on-line data is really just a function of the cost of the hardware. Utilizing standard "off-the-shelf" technology for disk storage modules, a capacity of 2,112 MB is easily attainable.

More important, however, than the total on-line data capacity is the rate at which the NAS processes the data. No matter how large the on-line capacity, it is obvious that if the NAS processing rate does not equal or exceed the input data rate, the on-line capacity will eventually be filled. Thus, we believe, immediate emphasis should be placed upon research necessary to totally automate the tasks of the NAS. Once this is accomplished, speed and on-line disk capacity could be adjusted to facilitate a smooth operation.

4.2 NAS HARDWARE

The DEC PDP 11/70 is an adequate machine for the present demands of an NAS. It may be in the future that the program and data space restrictions to 32K words of memory total will eventually prove to be a serious impediment. However, in this eventuality the NAS may be rather easily upgraded to a VAX 11/780 (see Section V), a virtual memory machine.

The NAS will access the on-line data files created by the RP both via the dual-ported disk storage modules and via the local network (see Section VI). One mode of operation would be to have the RP writing to one storage module, while the NAS reads from another already filled. An alternate way of operation is to have both the NAS and the RP accessing the same storage module with directory information (which is dynamically changing) transmitted over the local net. A third method of operation is to have all the data transmitted via the local network. This is practical if the network link has a high bandwidth and the RP is not too heavily loaded. Conceptually, this may seem to be the most elegant design, but practically its effectiveness will depend upon the RP's ability to feed the network at the required rate and perform its other functions. Our design is configured so that experiments may be conducted with any of these methods.

The NAS system as configured includes the existing E&S graphics system. The throughput to this peripheral processor can be made quite high via a DMA I/O port on each machine. The disk buffer storage of the E&S system could easily be increased to facilitate scrolling on the screen or the disk storage modules of the 11/70 could be used via the DMA access. More graphics processors of this type could easily be added to the system but it may be desirable to investigate other types of devices such as the storage scopes. These devices (like the Tektronix 4000 series) have been successfully used at high speed via a DMA port in seismic network analysis, notably at California Institute of Technology. These units have the advantage of high resolution and low cost compared to the E&S system at the price of some reduced graphics capability.

If there is a requirement for the NAS to send data such as the EWF to external sites, either an ARPANET IMP interface or (and) a regular communications channel could easily be configured in the system.

4.3 IMPLEMENTATION

A conservative approach to the development of the NAS is, in the first stage, simply to duplicate the software now on the NEP 40B on its replacement, the 11/70. This would be performed with special emphasis placed on eliminating those bottlenecks existing at present:

1. Recovering signal waveforms from tape.
2. Transfer of signal waveforms from 40B disks to limited 11/35 disk for display on E/S scope.
3. Reinitializing 11/35 system and recovery of disk data after a system crash.

As much as possible the NAS will work directly from disk data. However, the recovery of the signal waveforms

from the archived tapes will most likely be necessary for some time.

A second stage of development would clearly include experimentation with other types of graphics devices. We believe that several graphic stations should be configured "directly" into the NAS 11/70 system. There are many candidates for such graphic stations that span the technology from E&S type systems to the Tektronix storage scope type. The principal characteristics that are needed are the ability to display some 20 traces of about 2,400 points each (60 seconds at 40 samples/second) flicker free and the ability to scroll one or more traces independently. Writing speed should be high and DMA access to the 11/70 is clearly necessary. We recommend further research into these systems.

We further recommend that serious consideration be given to configuring the NAS with a VAX 11/780 as an upgrade to the 11/70 shown in the design, Figure 2.1 (see Section V).

V. THE RESEARCH SYSTEM

5.1 DESIGN PHILOSOPHY

The overall function of the SRC, as its name implies, is research. Thus, the research system (RS) is in many ways the most important element in the SRC design. Clearly, it is desirable to have the most powerful computing tool that can be afforded while at the same time maintaining compatability with the rest of the system. The only likely candidates for the RS, within the DEC 11 series line, are the 11/70 and the VAX 11/780. In our opinion, there is no doubt that the VAX is by far the more suitable computer. Introduced in 1977, it represents an upward extension of the 11 series. It is a true 32 bit machine. While the addressing modes and stack structures are similar to those of the 11 series, the 11/780 provides 32 bit addressing to give a large problem space, as well as 32 bit arithmetic and data paths for processing speed and accuracy.

5.2 COMPARISON BETWEEN THE 11/780 VERSUS THE 11/70

Figure 5.1 illustrates the basic architecture of the 11/70 and the 11/780. Table 5.1 provides a comparison of some of the main characteristics of the two processors. The significant differences are in:

1. The size of the cache.
2. The memory bus speed.
3. The program space.
4. The fact that the 11/70 has no writable control store.

Besides the obvious advantages of a 32 bit word, the chief increase in computing power (speed) is due to the memory

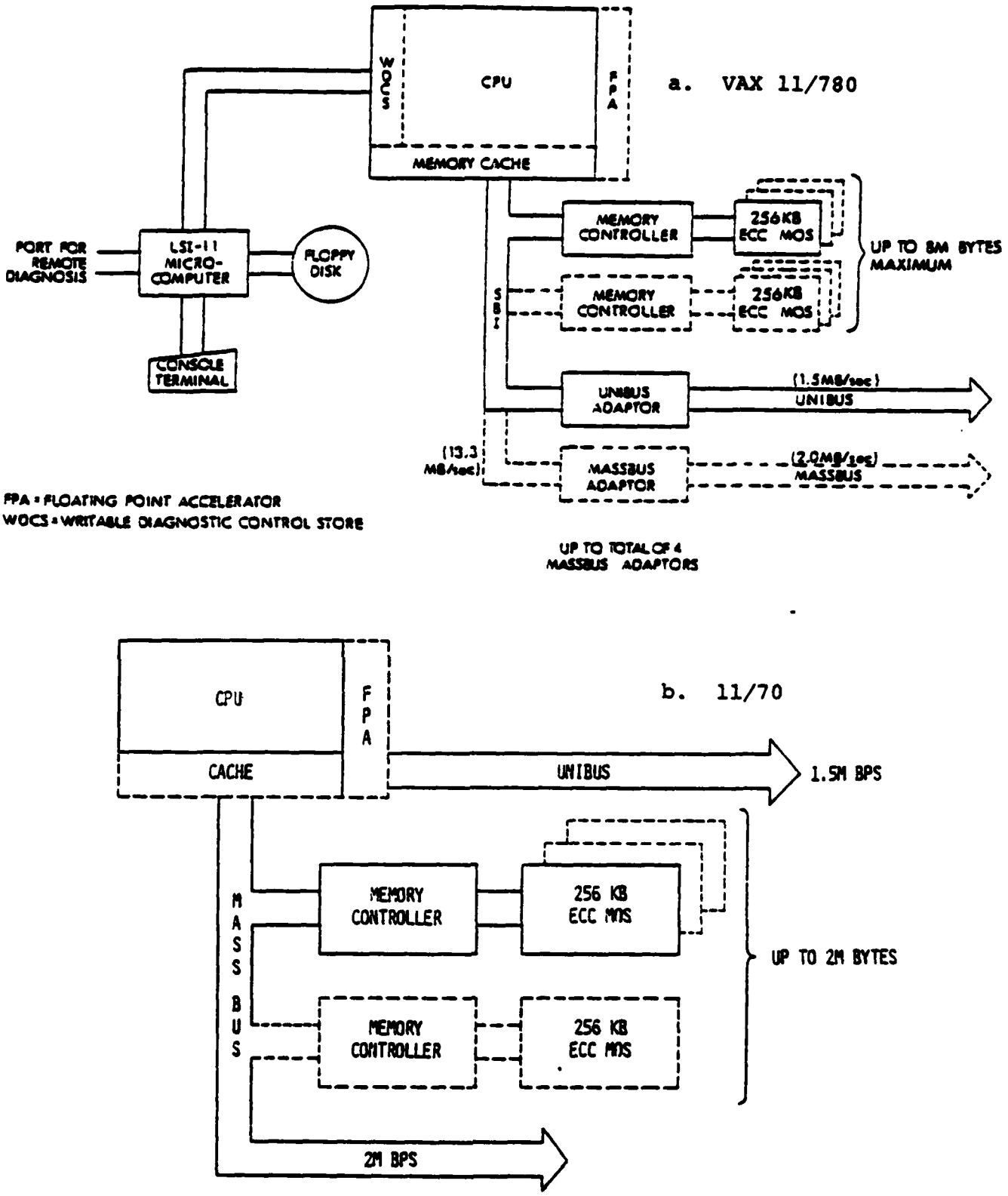


Figure 5.1. Architecture of the VAX 11/780 (a) and the 11/70 (b).

TABLE 5.1

PROCESSOR COMPARISON OF TWO CANDIDATE RESEARCH SYSTEM COMPUTERS

11/70	11/780
2 KB Cache	8 KB Cache
2 MB Memory	8 MB ECC MOS memory
32 bit FPA	32 bit FPA
32 bit memory path @ 2 MBPS	32 bit memory path @ 13.3 MBPS
16x16 bit general registers	16x32 bit general registers
64 KB program space	4 MB program space
No control store	12 KB writable control store
360 ns access time	290 ns access time

bus structure in the 11/780. It is the system's internal backplane and bus which conveys addresses, data and control information between the processor and memory, and between memory and peripheral controllers. In addition to its 13.3 Mbyte per second transfer rate, the bus provides an unusual degree of throughput and reliability because it uses:

1. Time-division multiplexing.
2. Distributed priority arbitration.
3. Parity and protocol checking on every transfer.
4. Transaction history recording.

The protocol, or sequence in which operations occur on the bus is time-division multiplexed to increase the effective bus bandwidth. Time-division multiplexing means that the transactions constituting one transfer operation are interleaved with the transactions constituting another transfer operation. Thus, several operations can be in progress over the same period of time. For example, the CPU can ask a memory controller to read some data; the same memory controller might then transfer previously requested data to an I/O device before transferring the required data to CPU.

In the 11/70, the processor bus may be tied up for the entire time required to complete a transfer because a requester acquires the bus to send an address and then keeps the bus while it waits for the requested data. In the 11/780, the bus is not held inactive during the data access time because bus ownership is relinquished after every cycle. A requester acquires the bus to send an address, relinquishes the bus, and then the responder acquires the bus to send the data. In the interim, any number of other transactions can be initiated or completed. This feature and the fact that transactions are buffered make it possible for the bus to operate at its full bandwidth, because a bus transaction can take place every 200 nanoseconds.

An idea of the relative computational power of these two systems and of the IBM 360/44 can be obtained from an arithmetically intensive benchmark we have run on these computers. The test consisted of a 16K Fast Fourier Transform (FFT) both forward and back. The time to complete the two transforms was:

IBM 360/44	PDP 11/70	VAX 11/780
97 sec	57 sec*	12 sec
	267 sec*	

From the hardware considerations, it is clear that the 11/780 is a superior machine for the RS. However, software must also be considered. It is desirable to run as much of the SRC as possible with the same software operating system. Fortunately, version seven of UNIX is now marketed by Western Electric and runs on both the 11/70 and the 11/780. A mini-UNIX is available for the 11/34 RP if so desired, however, its real time functions may require a different operating system such as DEC's RT-11.

Both the computer's manufacturer and the operating system's writers have gone to great length to insure the compatibility of the 11 series and the 11/780. Through the use of microcode, the 11/780 can operate in two modes: native or compatibility mode. In native mode the processor executes a large set of variable-length instructions, recognizes a variety of data types, and uses 16 32-bit general purpose registers. In compatibility mode the processor executes a set of PDP-11 instructions, recognizes integer data and uses eight 16-bit general purpose registers. While native mode is

---

*Since the program space in the 11/70 is 32K words, this test program would not fit on the machine. The 57 second result is the extrapolation of a 4K FFT result. The 267 second result is the 16K FFT run under the RSX-11M operating system using remapping.

the primary instruction execution state of the machine and compatibility mode the secondary stage, their instruction sets are very similar. A program can execute both native mode images and compatibility mode images.

As the native mode instruction set is a powerful extension of the PDP-11 instruction set, the programmer with previous PDP-11 knowledge who is developing new applications will experience a high level of adaptability. Similarly, 11/780 high-level languages are closely compatible with those of the PDP-11 family.

Under both the DEC operating system for the 11/780 and UNIX, almost total compatibility is insured. This means that in practice programs can be developed, debugged and run on the 11/780 and then down-loaded onto the 11/70. The only restriction of significance is the 11/70's limitation of 32K words of program space. As both the data formats and the file structures are common, data file transfers between machines are simple. Further, since the peripheral busses in the two machines are the same, MASSBUS and UNIBUS, peripherals can be common to both. In particular, dual-ported disks can be utilized. Finally, DEC has gone to some length to provide the full line of network peripherals (see Section VI) for the 11/780 so that it may be configured as shown in Figure 1.1 in the SRC. Indeed, several installations have been configured this way, notably one at the University of California, Berkeley, Computer Services Department, which uses the UNIX operating system.

The costs of an 11/70 system and an 11/780 system differ chiefly in the CPU and memory price. Using the DEC list price, we were quoted the following systems:

CPU
67 Mbyte Disc
45 IPS, 1,600 BPI Mag-Tape
8 Line Asynchronous Multiplexer

for $103K for the 11/70 version and $153K for the 11/780 version. Recently announced price reductions for memory will make both these prices lower. We believe the money is well spent. We recommend strongly that the VAX 11/780 be used as the RS computer. Indeed, if it is within the budgetary possibilities, we recommend using the 11/780 for both the NAS and the RS. Since the task of the NAS is only defined at present in concept, it too must be a research machine and it would be wise to endow it with as much power as the budget can afford.

VI. INTERPROCESSOR COMMUNICATION

6.1 LOCAL NETWORK DESIGN

The need for a local computer network for the SRC arises from two general requirements:

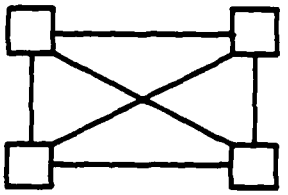
1. Access to a common data base by several processors.
2. Redundancy to provide reliability of the entire system.

There are a number of ways that local computers can be connected to form a network. The best system architecture for this application depends upon several factors, including:

1. Future expansion envisioned.
2. Degree of reliability required.
3. Budget.

The most general, and perhaps most desirable, arrangement is to achieve a fully distributed local network wherein every processor can communicate with every other processor. There are several ways to accomplish this goal, two of which are most applicable for the SRC.

1. The simplest system for a small number of computers is point-to-point connections. In this architecture, there is a separate path between each pair of machines. This provides for a simple to program, low-overhead and efficient system. The only drawback is that it takes $N(N-1)/2$ interconnections for N machines and, hence, for more than three or four computers it becomes expensive and cumbersome.



2. The second approach is to use what is essentially a loop structure. In this architecture each processor is connected in a Tee manner to a shared connecting link. The link can be a serial type connection or it can be a bus type parallel connection which achieves much higher transfer rates.

DEC offers hardware and software for both types of interconnections. In fact, they have a rather complete range of communications peripherals for the 11 series machines. For the point-to-point type of interconnection they offer both serial devices (DM11C) and parallel devices (DA11B), both of which can operate in a DMA mode to the connected processors. The chief difference is in transmission rates, the parallel connection being some five times faster (600 KBps).

For the common connecting line architecture, the PCL11-B utilizes a time multiplexed bus. The device is a UNIBUS peripheral which performs data transfers between computers using parallel transfers of 16 bit words on an interconnecting bus. It is a full duplex device so that one node can be both transmitting and receiving at the same time. Because of this and the multiplexed nature of the interconnect bus, up to all 16 possible conversations may be occurring concurrently. It performs the data transfers by direct memory access (DMA) with the computer memory and automatically performs error checking with hardware generated and checked word parity and CRC-16 block message checking.

The device manages its own protocol on the interconnect bus so as to completely manage the job of establishing communications with the intended recipient computer and passing, checking, and acknowledging the data message. Thus, use of it is essentially transparent to the user who simply directs the device to take a particular block of data or message of some specified length and sent it to the intended computer number N. No further user intervention is required until the PCL11-B I/O driver responds with either:

1. An I/O done indication after successful completion.
2. An I/O failure indication together with the reason, such as:
   -- Non-existent node
   -- Node busy after multiple retries
   -- Continued data errors after multiple retransmissions.

The PCL11-B UNIBUS interface consists of both a transmitter and receiver section as well as the electronics for timing and control of the interconnect bus. Redundant (dual) PCL11-B bus systems can be built as illustrated in Figure 6.1.

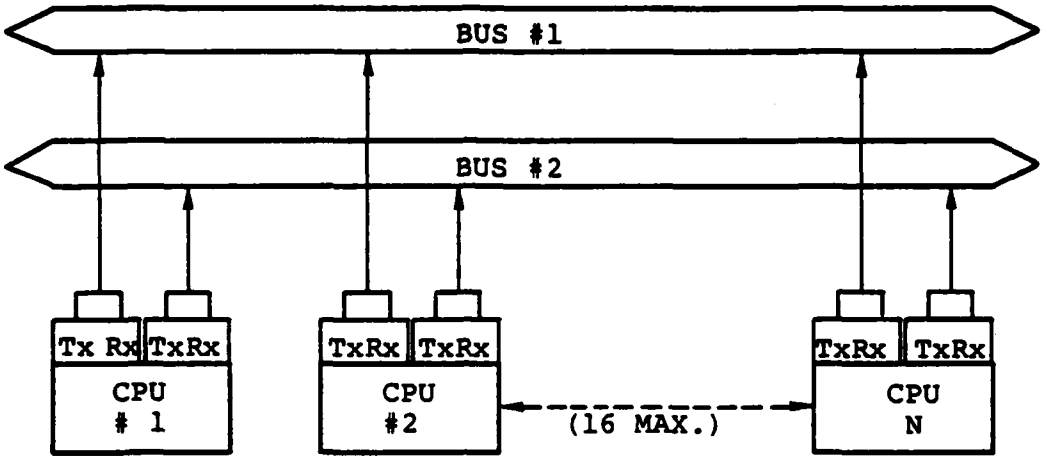


Figure 6.1. Redundant dual bus PCL11-B system.

This dual bus structure gives not only redundancy and back-up of the key interconnect mechanism, but increased power as well; since the two busses operate independently, they both can be used simultaneously.

The PCL11-B has been designed to provide certain features which are desirable for a very reliable system. Principally, due to its "Tee" structure (as oppossed to a "daisy chain" structure), individual CPUs can be powered down or disconnected from the network without ill effect. Further, each unit contains the logic for timing and control of the bus and in the event of a failure of the designated master timing unit, there can be automatic failover to a specific secondary unit. Any unit may be designated master or secondary.

The interconnect bus can transfer data at speeds up to one million bytes per second. The bus use can be allocated in either of two ways; the default method of equal use by the nodes in the network with "round robin" time slicing, or explicitly by means of a software loadable table in the device, giving the specific time slice sequence to be used -- up to a maximum of half the bus bandwidth to any one node. In this manner, the bandwidth of each node can be tuned to best meet the application need. For example, a data base management computer which receives short inquiry messages and transmits long data block responses could be set up to have a greater share of the bus bandwidth.

In summary, there are three standard network communications that can be considered:

1. DM11C: Point-to-point. 125 KBPS over serial triaxial cable to 2,000 m.
2. DA11B: Point-to-point. DMA transfers to 600 KBPS in half duplex.

3. PCL11-B: Multiple point. DMA transfers to multi-CPU bus up to IMBPS. Up to 16 processors on one bus.

Our recommendation for the local network link is the PCL11-B as it offers the highest throughput and is specifically designed for high reliability. A dual bus configuration may be considered to increase reliability.

6.2 SRC NETWORK HARDWARE

The SRC configuration shown in Figure 1.1 also utilizes dual-ported disk storage modules and there are two main reasons for this:

1. The reduction in cost resulting from the use of shared peripherals.
2. Advantage of dual-ported disks as a means of data base access over access via network link. When processor 2 accesses the disc, processor 1 experiences no interference, whereas when data is accessed via network, both processor's busses are tied up. The lack of bus contention during these data transfers via this method is considered to be a significant advantage in the SRC design.

We recommend that dual-ported disc storage modules be utilized particularly in the RP-NAS link where large quantities of data must be routinely transferred.

VII. SUMMARY AND FINAL RECOMMENDATIONS

This design for a Seismic Research Center has emphasized the role of research in configuring the system shown in Figure 1.1. We have considered the possible requirement that this system might have to act as an interim operational Seismic Data Center and our design is quite capable of so doing. However, the emphasis throughout was on computational power and flexibility rather than on reliability or redundancy. Nevertheless, the path to achieve these goals has been outlined.

We have stressed simplicity in the design using almost exclusively off-the-shelf components from Digital Equipment Corporation and Plessey Microsystems, both industry leaders. The lines of their equipment we chose are well developed, widely used and supported but yet still evolving. We believe that such choices will allow the SRC to evolve gracefully with the technology as new members of these product lines are introduced.

This design calls for the replacement of both IBM 360/40 mainframes with mini-computers and the elimination of the CCP. One result of utilizing this smaller and simpler computer architecture will be a considerable savings both in maintenance and operating costs -- savings that over a few years could easily exceed the cost of the equipment.

In summary, we make the following specific recommendations:

1. The SRC be configured with locally distributed processors consisting of:

   N Detection microprocessors,
   1 or 2 Recording processors,
   A network analysis system, and
   A Research system

   connected together in a local network.

2. An R&D project be initiated to test real-time detection algorithms in both the Plessey MIPROC-16 and the DEC LSI 11-23 micro-computers.

3. A PDP 11/34 be used as the recording processor with a second machine connected in parallel if redundancy is desired.

4. A PDP 11/70 or more preferably a VAX 11-780 be used as the network analysis system communicating with the RP both over the network link and via dual-ported disks.

5. A VAX 11/780 be used as the Research System.

6. The local network connecting all processors in the SRC utilize the DEC PCL11-B network bus (or similar hardware) with a dual bus structure used if redundancy is required.

A reasonable time table for the implementation of this design plan is illustrated in Figure 7.1.

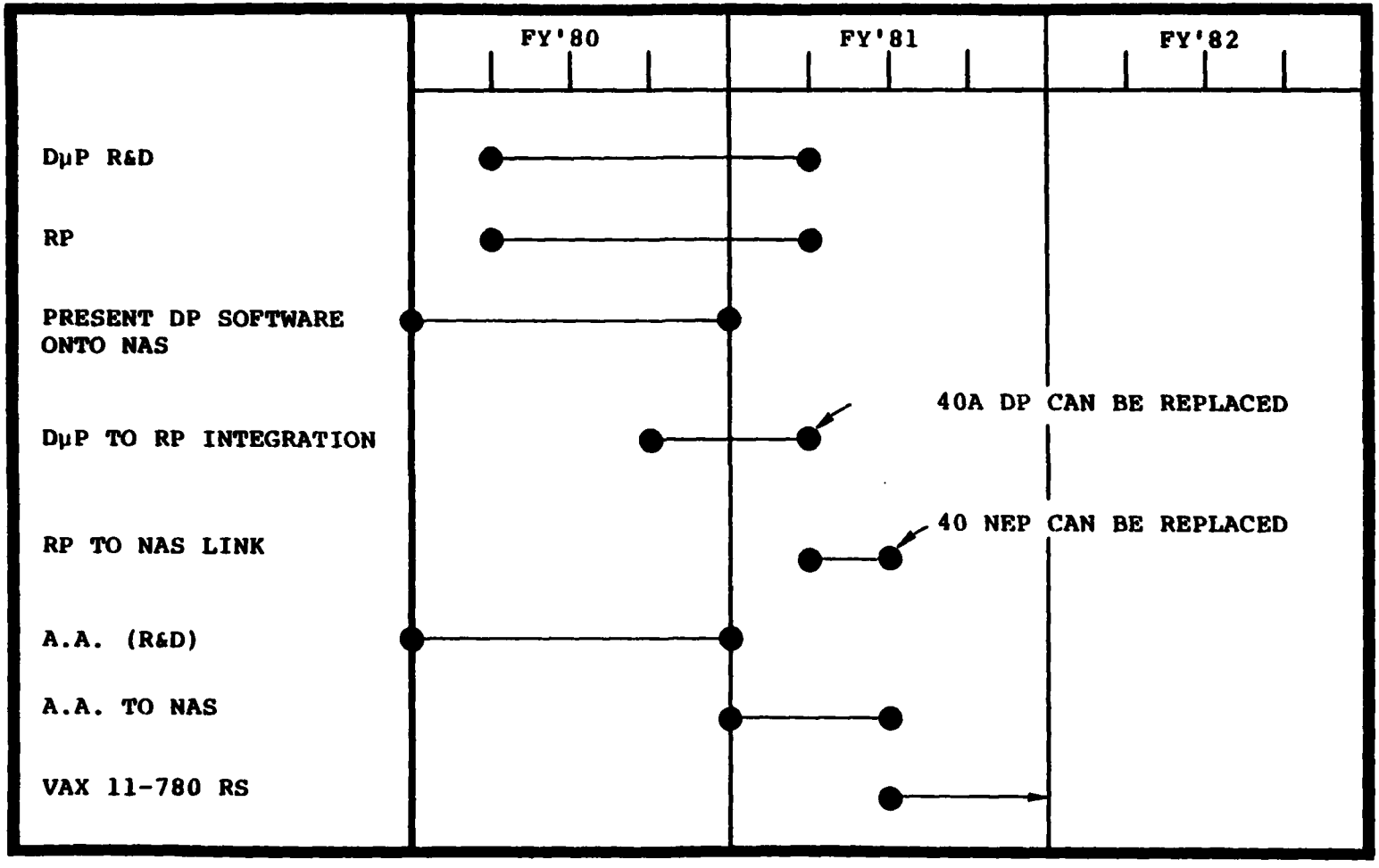


Figure 7.1. Seismic research center milestones.

REFERENCE

Chinnery, M. A. and R. G. North (1975), Science, 190, pp. 1197-1198.

APPENDIX A

MICROPROPROGRAMMABLE MICROPROCESSOR SURVEY

MANUFACTURER AND MODEL	ADVANCED MICRO DEVICES AM 2901A	AMERICAN MICROSYSTEMS (AMI) S9940	AMERICAN MICROSYSTEMS (AMI) S9900
PACKAGING			
Type	4-bit slice	16-bit CPU	16-bit CPU
Chip Technology	LP Schottky TTL	NMOS	NMOS
ARCHITECTURE & PERFORMANCE			
Data word size, bits	Any size,4-bit increments	16	16
Instruction word-size, bits	Varies	16	16
Clock frequency	To 8 MHz	1-5 MHz	3.3/4.4 MHz
Add time, register to register, microseconds per data word	0.15 (16 bits)	5	4.2/2.76
Number of instructions	Varies	72	69
General-purpose registers	17	16 + alternate workspace	16 + alternate 14 workspace
Number of directly addressable instruction words	Varies	2K	65K
INPUT OUTPUT CONTROL			
I/O word size, bits	Varies	1-16 bits	1-16 bits
SOFTWARE			
Resident assembler	No	Yes	Yes
Cross assembler	See comments below	Yes	Yes (time-share)
Higher-level language	No	Yes	Yes
Monitor or executive	No	Yes	Yes
PRICING & AVAILABILITY			
Price of basic CPU only (Quantity 100)	$14.70	NA	$31.25
Date of first delivery	July 1975	NA	NA
COMMENTS	Microprogram assembler (FORTRAN, PL/M), micro-programmable chip set for emulators; special purpose processors and controllers, all components available screened to MIL-STD-883 from stock.	-	Architecture of the S9900 family is memory-to-memory; operations occurring between registers can also be used on 2 memory locations.

MICROPROGRAMMABLE MICROPROCESSOR SURVEY

MANUFACTURER AND MODEL	AMERICAN MICROSYSTEMS (AMI) S9980/81	INTEL 8086	INTEL 8088
PACKAGING			
Type	16-bit CPU	16-bit CPU	8-bit CPU
Chip Technology	HMOS	HMOS	HMOS
ARCHITECTURE & PERFORMANCE			
Data word size, bits	16	8-16	8-16
Instruction word-size, bits	16	8-48	8-48
Clock frequency	10 MHz	5 MHz	5 MHz
Add time, register to register, microseconds per data word	0.8	0.6(8 or 16-bit)	0.6(8 or 16-bit)
Number of instructions	69	134	134
General-purpose registers	16 + alternate workspace	8 8 or 16-bit; 4 memory segmentation	8 8 or 16-bit; 4 memory segmentation
Number of directly addressable instruction words	16K	1 megabyte	1 megabyte
INPUT OUTPUT CONTROL			
I/O word size, bits	1-16 bits	8, 16	8
SOFTWARE			
Resident assembler	Yes	No	No
Cross assembler	Yes	Intellec MDS	Intellec MDS
Higher-level language	Yes	PLM-86	PLM-86
Monitor or executive	Yes	Yes	Yes
PRICING & AVAILABILITY			
Price of basic CPU only (Quantity 100)	NA	$112.50	NA
Date of first delivery	-	June 1978	April 1979
COMMENTS	-	Features 8 and 16-bit signed/unsigned arithmetic incl. multiply & divide; multiprocessor/coprocessor extension available; on-chip memory segmentation; multibus compatible.	Features 16-bit 8086 internal architecture; 8-bit 8085-compatible bus interface; software is compatible with 8086; 16-bit multiply/divide (signed and unsigned) multiprocessor/coprocessor extensions available.

SYSTEMS, SCIENCE AND SOFTWARE

MICROPROGRAMMABLE MICROPROCESSOR SURVEY

MANUFACTURER AND MODEL	INTEL 8089	MOTOROLA 2900 FAMILY	MOTOROLA 10800 FAMILY
PACKAGING			
Type	8/16-bit I/O processor	4-bit slice (ALU, sequencer, etc.)	4-bit slice (ALU, sequencer, etc.)
Chip Technology	HMOS	LS TTL	ECL
ARCHITECTURE & PERFORMANCE			
Data word size, bits	8-16	4/slice	4/slice
Instruction word-size, bits	16	Variable	Variable
Clock frequency	5 MHz	9.5 MHz (MC2901A)	Up to 12.5 MHz
Add time, register to register, microseconds per data word	-	143 nanoseconds (16 bits)	75 nanoseconds
Number of instructions	45	Unlimited	Unlimited
General-purpose registers	8 20-bit; 8 16-bit	16	6
Number of directly addressable instruction words	1 megabyte + 64K	Variable	Variable
INPUT OUTPUT CONTROL			
I/O word size, bits	8, 16	4-bit increments	4-bit increments
SOFTWARE			
Resident assembler	No	Yes, micro	Yes, micro
Cross assembler	Intellec MDS	No	No
Higher-level language	No	No	No
Monitor or executive	No	No	No
PRICING & AVAILABILITY			
Price of basic CPU only (Quantity 100)	NA	MC2901LC: $10.80 MC2901LM: $17.30	$30.00
Date of first delivery	June 1979	-	October 1975
COMMENTS	Features I/O-intensive instruction set; memory-based communication data structure between IOP and CPU; 1.25-megabyte transfer rate; intelligent DMA functions; multibus-compatible system interface.	Slice-type architecture; fully microprogrammed; can utilize any software; 16 on-chip registers (2901).	Slice-type microprocessor can be designed to utilize software from any system; 15 registers total, additional register files possible.

SYSTEMS. SCIENCE AND SOFTWARE

MICROPROGRAMMABLE MICROPROCESSOR SURVEY

MANUFACTURER AND MODEL	NATIONAL SEMICONDUCTOR IDM 2901A/A-1	NEC MICROCOMPUTERS μPD2901A	SIGNETICS 3002
PACKAGING			
Type	4-bit slice	4-bit polar slice	2-bit slice
Chip Technology	Bipolar	LP Schottky TTL	Bipolar Schottky
ARCHITECTURE & PERFORMANCE			
Data word size, bits	Multiples of 4 bits	4/slice	2 per slice
Instruction word-size, bits	9	Variable	Variable
Clock frequency	To 16 MHz	8 MHz	3 to 7 MHz
Add time, register to register, microseconds per data word	0.060	0.15/16 bits	0.25 to 0.6
Number of instructions	512	Variable	40+
General-purpose registers	17	77	10
Number of directly addressable instruction words	512	Variable	Variable
INPUT OUTPUT CONTROL			
I/O word size, bits	Multiples of 4 bits	Variable	2
SOFTWARE			
Resident assembler	No	No	No
Cross assembler	Yes	No	FORTRAN IV
Higher-level language	No	No	No
Monitor or executive	No	No	No
PRICING & AVAILABILITY			
Price of basic CPU only (Quantity 100)	$12.45	-	$20
Date of first delivery	September 1977	December 1978	July 1975
COMMENTS	Chip construction uses "SOL" (Schottky-ECL) technology which provides high speed and decreased power dissipation.	Lookahead carry, bus interface, microprogram sequencer, vectored interrupt controller available.	Control memory addressing by row & column; K-bus provides masking & bit testing; multiple bus structure; user-defined instruction set.

SYSTEMS, SCIENCE AND SOFTWARE

MICROPROGRAMMABLE MICROPROCESSOR SURVEY

MANUFACTURER AND MODEL	TEXAS INSTRUMENTS 74LS481
PACKAGING	
Type	4-bit slice
Chip Technology	Bipolar
ARCHITECTURE & PERFORMANCE	
Data word size, bits	4
Instruction word-size, bits	17
Clock frequency	10 MHz; 8 MHz
Add time, register to register, microseconds per data word	0.10; 0.13
Number of instructions	User-defined
General-purpose registers	2
Number of directly addressable instruction words	-
INPUT OUTPUT CONTROL	
I/O word size, bits	Dual 4-bit ports
SOFTWARE	
Resident assembler	-
Cross assembler	-
Higher-level language	-
Monitor or executive	-
PRICING & AVAILABILITY	
Price of basic CPU only (Quantity 100)	-
Date of first delivery	1st quarter 1977
COMMENTS	Full parallel, dual input/output ports; performs a 16-bit by 16-bit double-precision division in less than 3 microseconds.

SYSTEMS, SCIENCE AND SOFTWARE

APPENDIX B

MICROPROGRAMMABLE MICROCOMPUTER SURVEY

MANUFACTURER AND MODEL	ALPHA MICROSYSTEMS AM 100	COMPUTER AUTOMATION NAKED MINI LSI-4/10	COMPUTER AUTOMATION NAKED MINI LSI-4/30
MICROPROCESSORS			
Technology	NOS	LSI	MSI
Data word size, bits	8 or 16	8 or 16	8 or 16
Instruction word size, bits	16	16	16
Clock frequency	2 Or 3.3 MHz	5 MHz	4 MHz
Add time, register to register, microseconds per data word	7	3.10	1.10
Number of instructions	150	89 (+ 38 optional)	104 (+ 24 optional)
Total number of registers	8	8	8
RANDOM-ACCESS MEMORY	Optional	Optional	Optional
Capacity, bytes	48K to 16M	512K	512K
Cycle time, nanoseconds	500	556	556
READ-ONLY MEMORY	Boot load only	Optional	Optional
Capacity, bytes	2K	32K	32K
Cycle time, nanoseconds	500	1400	1400
PROGRAMMABLE ROM	Optional	Optional	Optional
Capacity, bytes	16K	32K	32K
Cycle time, nanoseconds	500	1400	1400
INPUT/OUTPUT CONTROL			
I/O word size, bits	8	8 or 16	8 or 16
Number of I/O channels	256	4 to 64	4 to 64
Max I/O rate, words/sec.	2 million	1.1 MB	1.8 MB
SOFTWARE			
Resident assembler	Yes	Yes	Yes
Cross assembler	no	Naked Mini LSI-2	Naked Mini LSI-2
Higher-level language	BASIC, FOR., PASC.	FORTRAN	FORTRAN
Monitor or executive	Yes	Yes	Yes
	No		
PRICING & AVAILABILITY			
Price of basic system with 1K words of RAM	$1,500	$520	$1,395 (8K RAM)
Date of first delivery	April 1976	May 1977	May 1977
COMMENTS	Multi-taking time-sharing system for S100 bus users.	Alpha 4/10 packaged systems available.	Alpha 4/30 packaged systems available.

SYSTEMS, SCIENCE AND SOFTWARE

MICROPROGRAMMABLE MICROCOMPUTER SURVEY

MANUFACTURER AND MODEL	COMPUTER AUTOMATION NAKED MINI LSI-4/90	DETECTION SCIENCES, INC. SYSTEM 8-MBE	DETECTION SCIENCES, INC. SYSTEM 8-MBA
MICROPROCESSORS			
Technology	MSI	Bipolar	Bipolar
Data word size, bits	8 or 16	8	8
Instruction word size, bits	16	8 to 24	8 to 24
Clock frequency	4 MHz	4 MHz	4 MHz
Add time, register to register, microseconds per data word	1.75	N/A	1.25
Number of instructions	117 (+ 26 optional)	User-determined	134
Total number of registers	8	User-determined	104
RANDOM-ACCESS MEMORY	Optional	---	---
Capacity, bytes	512K	65K	64K
Cycle time, nanoseconds	550	350 to 1000	350 to 1000
READ-ONLY MEMORY	Optional	---	Optional
Capacity, bytes	32K	65K	64K
Cycle time, nanoseconds	1400	250	250
PROGRAMMABLE ROM	Optional	---	---
Capacity, bytes	32K	65K	64K
Cycle time, nanoseconds	1400	750	750
INPUT/OUTPUT CONTROL			
I/O word size, bits	8 or 16	8	8
Number of I/O channels	4 to 64	256	256
Max I/O rate, words/sec.	1.8 MB	2 million	2 million
SOFTWARE			
Resident assembler	Yes	No	No
Cross assembler	Naked Mini LSI-2	Yes	Yes
Higher-level language	FORTRAN	Yes	Yes
Monitor or executive	Yes	Yes	Yes
PRICING & AVAILABILITY			
Price of basic system with 1K words of RAM	$2,890 (8K RAM)	$1,950	$1,650
Date of first delivery	May 1977	October 1975	February 1975
COMMENTS	Alpha 4/90 packaged systems available.	Formerly Warner and Swasey Co.	Formerly Warner and Swasey Co.

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MICROPROGRAMMABLE MICROCOMPUTER SURVEY

MANUFACTURER AND MODEL	DIGITAL EQUIPMENT LSI-11	DIGITAL EQUIPMENT LSI11-23	ELECTRONIC PRODUCTS ASSOCIATES MICRO-68b
MICROPROCESSORS			
Technology	NMOS	NMOS	NMOS
Data word size, bits	16	16	8
Instruction word size, bits	16, 32, 48	16, 32, 48	8, 16, 24
Clock frequency	3 MHz	---	Up to 1.5 MHz
Add time, register to register, microseconds per data word	3.5	1.8 (est.)	1.33
Number of instructions	80	80	72
Total number of registers	8	8	6
RANDOM-ACCESS MEMORY	---	MOS	
Capacity, bytes	8K up to 64K	256K	64K
Cycle time, nanoseconds	400	400 ns	450
READ-ONLY MEMORY	---		
Capacity, bytes	8K up to 64K		1K
Cycle time, nanoseconds	400		450
PROGRAMMABLE ROM	---		
Capacity, bytes	8K up to 64K		Up to 16K
Cycle time, nanoseconds	400		450
INPUT/OUTPUT CONTROL			
I/O word size, bits	16	16	16
Number of I/O channels	Common bus	Common Bus	2
Max I/O rate, words/sec.	833K	833K words/sec	375K
SOFTWARE			
Resident assembler	Yes	Yes	Yes
Cross assembler	DECsystem-10	Yes	Yes
Higher-level language	FORTRAN, BASIC	FORTRAN/BASIC	Yes
Monitor or executive	RT-11, RSX-11S	RT11, RSX11M	Yes
PRICING & AVAILABILITY			
Price of basic system with 1K words of RAM	$990 (with 4K)	?	$1,878 (8K words of RAM)
Date of first delivery	April 1975	1979	December 1976
COMMENTS	PDP-11 compatible, with 11/40 instruction repertoire and RT-11 and RSX-11 support.	18-bit address, F.P. hardware, memory management.	Complete development system available.

MICROPROGRAMMABLE MICROCOMPUTER SURVEY

MANUFACTURER AND MODEL	HARRIS SEMICONDUCTOR MICRO-12 HS6610D8-01	PCM, INC. PCM - 12A	PLESSEY MICROSYSTEMS MIPROC-16
MICROPROCESSORS			
Technology	CMOS	CMOS	Schottky, bipolar
Data word size, bits	12	12	16
Instruction word size, bits	12	12	16
Clock frequency	2.5 MHz	4.0 MHz	4 MHz
Add time, register to register, microseconds per data word	8	5.0	0.250
Number of instructions	70+	76	100
Total number of registers	2	6	4
RANDOM-ACCESS MEMORY	Standard	Optional	---
Capacity, bytes	4K	32K	64K
Cycle time, nanoseconds	---	300	100
READ-ONLY MEMORY	Standard	No	---
Capacity, bytes	4K	---	64K
Cycle time, nanoseconds	2	---	70
PROGRAMMABLE ROM	No	Optional	---
Capacity, bytes	---	32K words	64K
Cycle time, nanoseconds	---	1000	70
INPUT/OUTPUT CONTROL			
I/O word size, bits	12	12	16
Number of I/O channels	3	64 (bus organized)	256
Max I/O rate, words/sec.	---	2M	1.5M
SOFTWARE			
Resident assembler	No	Yes	No
Cross assembler	Yes, DEC PDP-8	No	FORTRAN IV/PDP-11
Higher-level language	No	Yes	PL-Miproc
Monitor or executive	Yes	Yes	Yes
PRICING & AVAILABILITY			
Price of basic system with 1K words of RAM	$650	$699 (kit w/o memory) $933 (w/4K memory)	$1,900
Date of first delivery	August 1978	December 1975	January 1976
COMMENTS	Implements PDP-8 instruction set, 4K x 12 CMOS memory board available; system is also available in kit form.	Software-compatible with DEC PDP-8 family; CMOS and dynamic RAM memory also available; Firmware bootstrap loader standard.	Fast machine rated at 4 MIPS; MIL version available.

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MICROPROGRAMMABLE MICROCOMPUTER SURVEY

MANUFACTURER AND MODEL	TEXAS INSTRUMENTS 9900/4	TEXAS INSTRUMENTS TM 9900/100M	TEXAS INSTRUMENT TM 990/101M
MICROPROCESSORS			
Technology	NMOS	NMOS	NMOS
Data word size, bits	8, 16	16	16
Instruction word size, bits	16, 32, 48	16-48	16-48
Clock frequency	2 MHz	3MHz	3 MHz
Add time, register to register, microseconds per data word	7.33	4.6	4.6
Number of instructions	69	4.6	69
Total number of registers	19 (see Comments)	16 (see Comments)	16 (see Comments)
RANDOM-ACCESS MEMORY	Standard	Standard	Standard
Capacity, bytes	8K, 16K up to 64K	Up to 64K	Up to 64K
Cycle time, nanoseconds	650	450	450
READ-ONLY MEMORY	Standard	Standard	Standard
Capacity, bytes	32K	Up to 64K	64K
Cycle time, nanoseconds	660	450	450
PROGRAMMABLE ROM	Standard	Standard	Standard
Capacity, bytes	8K, 16K up to 64K	64K	64K
Cycle time, nanoseconds	650	450	450
INPUT/OUTPUT CONTROL			
I/O word size, bits	1-16	1-16	1-16
Number of I/O channels	4,096	4,096	4,096
Max I/O rate, words/sec.	1.6M (DMA)	---	---
SOFTWARE			
Resident assembler	Yes	Yes	Yes
Cross assembler	IBM 370	Universal 16-bit package	Universal 16-bit package
Higher-level language	FORTRAN	BASIC, Pascal	BASIC, Pascal
Monitor or executive	Standard: 2 monitors	Yes	Yes
PRICING & AVAILABILITY			
Price of basic system with 1K words of RAM	$800	$450 (256 words RAM)	$625
Date of first delivery	March 1976	June 1977	April 1978
COMMENTS	Any number of 16-register files can be defined in memory; multiply/divide hardware; memory-to-memory instructions.	Any number of 16-register files can be defined in memory.	Any number of 16-register files can be defined in memory.

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MICROPROGRAMMABLE MICROCOMPUTER SURVEY

MANUFACTURER AND MODEL	TEXAS INSTRUMENTS TM 990/180M
MICROPROCESSORS	
Technology	NMOS
Data word size, bits	8
Instruction word size, bits	16-48
Clock frequency	2.5 MHz
Add time, register to register, microseconds per data word	8.8
Number of instructions	69
Total number of registers	16 (see Comments)
RANDOM-ACCESS MEMORY	Standard
Capacity, bytes	Up to 16K
Cycle time, nanoseconds	450
READ-ONLY MEMORY	Standard
Capacity, bytes	16K
Cycle time, nanoseconds	450
PROGRAMMABLE ROM	Standard
Capacity, bytes	16K
Cycle time, nanoseconds	450
INPUT/OUTPUT CONTROL	
I/O word size, bits	1-16
Number of I/O channels	2,048
Max I/O rate, words/sec.	---
SOFTWARE	
Resident assembler	Yes
Cross assembler	Universal 16-bit package
Higher-level language	None
Monitor or executive	Yes
PRICING & AVAILABILITY	
Price of basic system with 1K words of RAM	$435 (256 words RAM)
Date of first delivery	June 1977
COMMENTS	*Any number of 16-register files can be defined in memory.*

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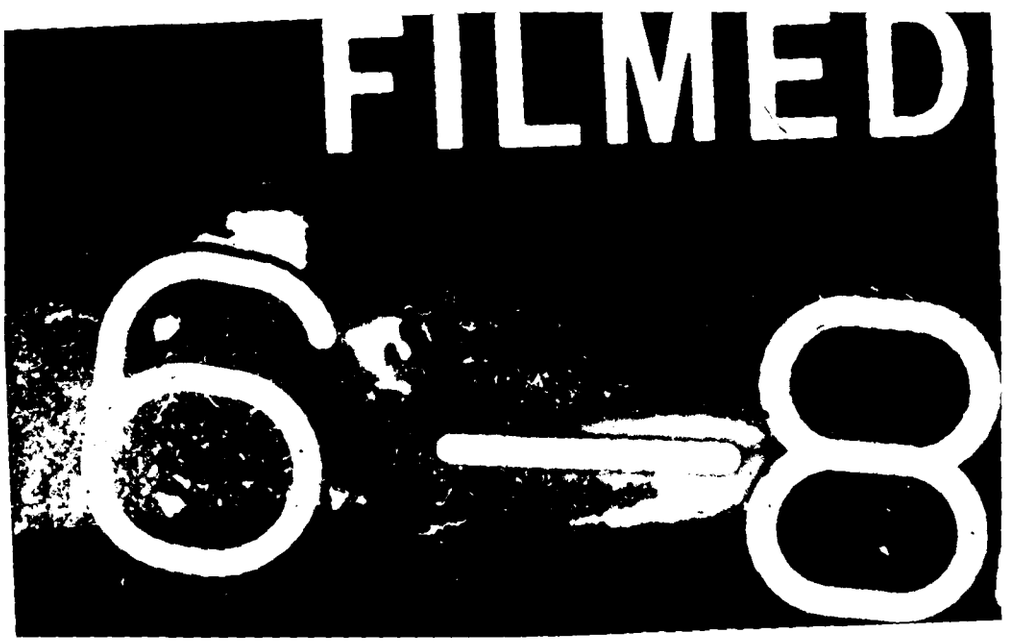
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